UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/768,271	01/25/2001	Tsukasa Yajima	PNET.009D	3802

20987 7590 08/09/2005

VOLENTINE FRANCOS, & WHITT PLLC
ONE FREEDOM SQUARE
11951 FREEDOM DRIVE SUITE 1260
RESTON, VA 20190

EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 08/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/768,271	YAJIMA, TSUKASA	
	Examiner	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-9 and 11-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *6-9 and 11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/02/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed July 22, 2005 has been entered. Claims 6, 11, 14 and 16 have been amended. Claims 6-9 and 11-19 are pending.

Change of Correspondence Address

2. The notice of changing address filed July 26, 2005 is acknowledged.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on June 2, 2005 was filed after the mailing date of the Non-Final Office Action on April 22, 2005. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

4. Claims 6-9 and 11-19 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "whereby edges of said protective layer are not covered by sidewalls spacers" (as recited in amended claims 1, 11 and 16) in the application as filed.

Since the drawing is only an illustration of the invention, a limitation of the claim must have support in the original specification.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 6-9 and 11-19 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The term "whereby edges of said protective layer are not covered by sidewall spacers " is a negative limitation that renders the claims indefinite because it was an attempt to claim the invention by excluding what the inventor *did not invent* rather than distinctly and particularly pointing out what they did invent. See *In re Schechter*, 205 F.2d 185, 98 USPQ 144 (CCPA 1953). (See MPEP 2173.05(i)). Any negative limitation or exclusionary proviso *must have* basis in the original disclosure. See *In re Johnson*, 558 F.2d 1008, 1019, 194 USPQ 187, 196 (CCPA 1977).

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 6-9, 11-13 and 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Hotta (U.S. Patent No. 5,418,179).

With respect to claim 6, as best understood by the examiner, Hotta teaches a semiconductor device as claimed including:

first (111) and second (116) gates formed on an active regions (103, 104) of a substrate (101), the first and second gates each consisting of a refractory metal layer (113) on a polysilicon layer (112);

a field oxide (105) formed on the substrate (101) between the first (111) and second gate (116);

side walls formed on side surfaces of the first (111) and second gates (116), the side walls being a silicon oxide film (122);

a protective layer (120) formed selectively on the field oxide (105) to prevent overetching of the field oxide,

the protective layer (120) being a conductive layer and having an edge thereof on the field oxide (105), whereby edges of the protective layer are not covered by sidewall spacers; and

an insulating layer (122), a contact hole, and a connecting wire (126) formed above the surface of the substrate (101). (See Fig. 5).

Product by process limitation:

The expression "to prevent overetching of said field oxide" (claims 6, 11 and 16) is taken to be a product by process limitation and is given no patentable weight. A product by process claim directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See *In re Fessman*, 180 USPQ 324, 326 (CCPA 1974); *In re Marosi et al.*, 218 USPQ 289, 292 (Fed. Cir. 1983); and particularly *In re Thorpe*, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make it clear that it is the patentability of the final structure of the product "gleaned" from the process steps, which must be determined in a "product by process" claim, and not the patentability of the process. See also MPEP 2113. Moreover, an old and obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

Note that, since the protective layer (120) of Hotta is formed on the field oxide (105) and is preventing overetching of the field oxide. (See Fig. 7B).

The above also applies to claims 11 and 16 as well.

With respect to claim 11, as best understood by the examiner, Hotta teaches a semiconductor device as claimed including:

a gate (116) formed on an active region (104) of a substrate (101);

a field oxide (105) formed on the substrate adjacent the active region (104);

a protective layer (120) formed on the field oxide (105) to prevent overetching of the field oxide;

the protective layer (120) being a conductive layer and having an edge thereof on the field oxide (105), whereby edges of the protective layer are not covered by sidewall spacers; and

an insulating layer (122), a contact hole, and a connecting wire (126) formed above the surface of the substrate (101),

the protective layer (120) being formed on the field oxide (105) only. (See Fig. 5).

With respect to claims 7 and 12 the protective layer (120) of Hotta is a polysilicon layer.

With respect to claim 8, the protective layer (120) of Hotta is formed on the field oxide (105) only.

With respect to claims 9 and 13, the gates (111, 116) of Hotta are a MOSFET gate.

With respect to claim 15, the semiconductor device of Hotta further comprising an additional gate (111) formed on the substrate (101), the field oxide (105) being formed on the substrate (101) between the gate (116) and the additional gate (111).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 16-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta '179 in view of Applicant Admitted Prior Art (AAPA).

With respect to claim 16, as best understood by the examiner, Hotta teaches a semiconductor device substantially as claimed including:

a gate (116) formed on an active region (104) of a substrate (101), the gate (116) consisting of a refractory metal layer (118) on a polysilicon layer (117);

a field oxide (105) formed on the substrate (101) adjacent the active region (104);

a protective layer (120) formed on the field oxide (105) to prevent overetching of the field oxide,

the protective layer (120) being a conductive layer and having an edge thereof on the field oxide (105), whereby edges of the protective layer are not covered by sidewall spacer; and

an insulating layer (122), a contact hole, and a connecting wire (126) formed above the surface of the substrate (101),

the protective layer (120) being formed on the field oxide (105) only. (See Fig. 5).

Thus, Hotta is shown to teach all the features of the claim with the exception of forming sidewall spacers on side surface of the gate.

However, AAPA teaches a semiconductor device including sidewall spacers (37) are formed on side surface of gate (35). (See Fig. 2F).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form sidewall spacers on side surface of the gate of Hotta as taught by AAPA to prevent contact hole cut into the gate, thus short circuit may be prevented. This matter is well known in the art.

With respect to claim 17, the protective layer (120) of Hotta is a polysilicon layer.

With respect to claim 18, the gate (116) of Hotta is a MOSFET gate.

With respect to claim 19, the semiconductor device of Hotta further comprising an additional gate (111) formed on the substrate (101), the field oxide (105) being formed on the substrate between the gate (16) and the additional gate (111).

8. Claim 14 is rejected under 35 U.S.C. 103(a) as being unpatentable over Hotta '179 as applied to claim 11 above, and further in view of AAPA.

With respect to claim 14, Hotta teaches a semiconductor device as described in claim 11 above including an insulating layer formed above the surface of the substrate.

Thus, Hotta is shown to teach all the features of the claim with the exception of forming sidewall spacers on side surface of the gate.

However, AAPA teaches a semiconductor device including sidewall spacers (37) are formed on side surface of gate (35), thus, the insulating layer subsequently formed on the substrate would have cover the gate and the sidewall spacers as well. (See Fig. 2F).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form sidewall spacers on side surface of the gate of Hotta as taught

by AAPA to prevent contact hole cut into the gate, thus short circuit may be prevented. This matter is well known in the art.

Response to Arguments

9. Applicant's arguments filed July 22, 2005 have been fully considered but they are not persuasive.

Regarding the term "side walls" and "sidewall spacers", it is well known in the art that any element, layer, structure, etc., has an edge then that edge is a side wall. However, the structure like element 37 of AAPA, is known in the art to be sidewall spacers.

One having ordinary skill in the art should no be confused between "side walls" and "sidewall spacers".

Regarding the new matter, rejection under 35 U.S.C 112, first paragraph, Applicant appears to contend that if the drawing does not include any element, the applicant can exclude that element by claiming "do not have such and such" as in the amended claims.

However, MPEP 2173.05 (i) made it very clear that by claiming "whereby edges of said protective layer **are not covered** by sidewall spacers", applicant is attempted to claim what he has **not** invented.

Technically speaking, going from Fig. 1g to Fig. 1h, one having ordinary skill in the art should recognize that forming spacers 37 by etching the oxide layer 35 also results

in forming oxide spacers on the edges of the protective layer 12 as well. (See Yoo 5,605,853).

The rejections under 35 U.S.C. 112, first and second paragraphs, are maintained.

10. Applicant's arguments with respect to the amended claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ANH D. MAI
PRIMARY EXAMINER